Docket No.: M4065.0985/P985
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Chandra Mouli

Application No.: 10/680,158 Confirmation No.: 5806

Filed: October 8, 2003 Art Unit: 2814

For: 1T/0C RAM CELL WITH A WRAPPED-AROUND GATE DEVICE STRUCTURE Examiner: H. Weiss

APPELLANT'S REPLY BRIEF UNDER 37 C.F.R. § 41.41

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is filed pursuant to 37 C.F.R. § 41.41 and is responsive to the Examiner's Answer mailed April 26, 2007 in connection with the appeal from the final rejection of claims 1-67 in the above-identified U.S. patent application.

I. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 67 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 0
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 1-67
4. Claims allowed: 0
5. Claims rejected: 1-67

C. Claims On Appeal

The claims on appeal are claims 1-67

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 and 62-67 under 35 U.S.C. 103(a) as being unpatentable over "Memory Design Using One-Transistor Gain Cell on SOI" by Ohsawa et al. (2002 IEEE International Solid State Circuits Conference) ("Ohsawa") (attached as Exhibit 1 in Appendix B) in view of U.S. Patent No. 6,838,322 to Pham et al. ("Pham") (attached as Exhibit 2 in Appendix B), and further in view of U.S. Patent No. 6,313,486 to Kencke et al. ("Kencke") (attached as Exhibit 3 in Appendix B).

B. The rejection of claims 8 and 35 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 5,448,513 to Hu et al. ("Hu") (attached as Exhibit 4 in Appendix B).

C. The rejection of claims14-16, 38-40 and 59-61 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 6,806,537 to Matsumoto et al. ("Matsumoto") (attached as Exhibit 5 in Appendix B).

D. The rejection of claims 15 and 58 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 5,307,305 to Takasu (attached as Exhibit 6 in Appendix B).

E. The rejection of claims 15 and 58 under 35 U.S.C. 103(a) as being unpatentable over Ohsawa, Pham, Kencke and further in view of U.S. Patent No. 6,221,724 to Yu et al. ("Yu") (attached as Exhibit 7 in Appendix B).

III. ARGUMENT

Although the Examiner's Answer does not raise any new grounds for rejection, Appellant writes briefly here to respond to the Examiner's remarks regarding Appellant's arguments in the Appeal Brief.

A. CLAIMS 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 AND 62-67 ARE PATENTABLE OVER OHSAWA IN VIEW OF PHAM AND FURTHER IN VIEW OF KENCKE (GROUND OF REJECTION A).

1. Ohsawa is relied on for the disclosure of a "storage transistor," and Pham is relied on for the disclosure of a "gate structure at least partially wrapping around the body portion", but there is no convincing obviousness analysis and no motivation to combine the two references.

a. It would not be obvious to combine Ohsawa with Pham because there is no disclosure, teaching or suggestion in Ohsawa or Pham to use the FinFET of Pham as a storage transistor

Each of claims 1-7, 11, 12, 17-21, 23, 24, 28-34, 37, 41-53, 56, 57 and 62-67 recite a storage transistor having a gate structure wrapping at least partially around a body portion (as described above in Section V). The Examiner's Answer, admits, at p. 4, that Ohsawa does not "show the storage transistor as a FinFET with a gate structure wrap[ping] around the body portion in at least two planes and consisting of a plurality of gates," and goes on to state that it would have been obvious to combine the FinFET of Pham with the storage transistor of Ohsawa.

The Supreme Court recently held in *KSR Int'l Co. v. Teleflex Inc.* that "the [Graham] factors continue to define the inquiry that controls" a finding of obviousness and reiterated that a "patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." 127 S. Ct. 1727, 1734 (U.S. 2007). The Graham factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966).

Appellant submits that the Examiner has not properly shown that the Appellant's claims would have been obvious by conducting an examination of the Graham factors. "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." *MPEP* 2141. Instead, as evidence that Ohsawa and Pham may be properly combined and that the Appellant's claims are obvious in light of these references, the Examiner merely stated that it would be obvious to combine the FinFET of Pham in the device of Ohsawa "to obtain suitable threshold voltages for high-speed logic devices while controlling extrinsic resistance." Examiner's Answer at p. 4. This statement is not an adequate substitution for an analysis of the Graham factors and does not show obviousness.

Furthermore, the Examiner's statement is not even convincing as evidence of motivation to combine Ohsawa and Pham because it is taken out of context and because there is no support in either Ohsawa or Pham that combining the FinFET of Pham with the device of Ohsawa would provide any benefit. The statement that the Examiner relies on for motivation is made by Pham while describing the drawbacks of prior art (double gated MOSFET technology) where Pham states that "[a] significant limitation of this technology, however, relates to the inability of these designs to obtain suitable threshold voltages for high-speed logic devices while controlling extrinsic resistance" and does not actually describe the benefits of Pham's FinFET.

Furthermore as discussed in the Appeal Brief at page 12, Pham only discloses a transistor used to *transfer* charge. There is no suggestion in Pham that the disclosed FinFET could be used to *store* charge. Proper analysis under the Graham factors reveals that this difference between the disclosure of Pham and the claims at issue renders Pham non-analogous art. Pham does not teach or suggest that any of the advantages of the FinFET taught by Pham would be advantageous to or could be incorporated by a storage transistor, such as the one taught by Ohsawa. Absent Appellant's disclosure, the Examiner's Answer has not shown any evidence that, at the time the invention was made, that a FinFET or other similar transistor having a gate structure which at least partially wraps around a body portion can be employed as a storage device nor how it would be obvious to modify such a device to do so.

The conclusory statement and sparse reasoning provided by the Examiner are not enough to maintain a finding that the Appellant's claims are obvious. "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* at 722, citing *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006). In light of the holding of *KSR* and in light of the lack of any convincing argument as to the obviousness of the Appellant's claims, Appellant respectfully submits that this rejection is based improperly on hindsight and should be reversed.

b. Secondary considerations show that the Appellant's claims are unobvious because Pham teaches away from the use of FinFET as a storage transistor and there is no evidence that the combination of Pham with Ohsawa would be functional.

In *KSR*, the Court reiterated the importance of secondary considerations to the Graham factors, when it cited with approval its own holding in *United States v. Adams*, 383 U.S. 39, 40, 86 S. Ct. 708, 15 L. Ed. 2d 572, 174 Ct. Cl. 1293 (1966), in which the Court "relied upon the corollary principle that when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." *Id.* at 720.

The Appellant has shown that Pham teaches away from the use of the disclosed FinFET as a storage transistor in the Appeal Brief at pages 13-15 because combining the FinFET of Pham with the storage transistor of Ohsawa would result in a seemingly inoperable device. The Examiner's Answer has not provided any evidence that the combination of the FinFET of Pham with the storage transistor of Ohsawa would result in an operable or even seemingly operable device. However, the Examiner's Answer does provide some rebuttal arguments to the Appellant's arguments of inoperability, which the Appellant will now address.

The Examiner states that "the Appellant repeatedly invokes unclaimed limitations "channel doping" and "carrier mobility" as evidence that Pham et al. does not teach the use of the FinFET as a storage transistor." This statement is incorrect. Appellant invokes arguments regarding channel doping and carrier mobility as evidence that "the changes proposed by the Final Rejection would destroy the ability of the FinFET of Pham to operate as contemplated by the Pham disclosure." Appeal Brief, pages 13-14. It is, however, true that Pham does not teach the use the FinFET as a storage transistor.

The Examiner argues that ""channel doping" does not appear as a limitation in any of the pending claims and, therefore, should not be considered as a basis of establishing the legitimacy of combining the prior art." Examiner's Answer, page 8. Nowhere in the Examiner's Answer is the Examiner's reliance on the improper use of hindsight reasoning more clearly evident than in this statement. By focusing so intently on the Appellant's claims, the Examiner has wrongly implied that the content of the Appellant's claims dictates whether combining the FinFET of Pham with the device of Ohsawa would result in an operable device. Obviously, this implication is false, because Appellant's claims have no bearing on the principles of electron transport through doped or undoped silicon nor, indeed, on the principles of physics in general.

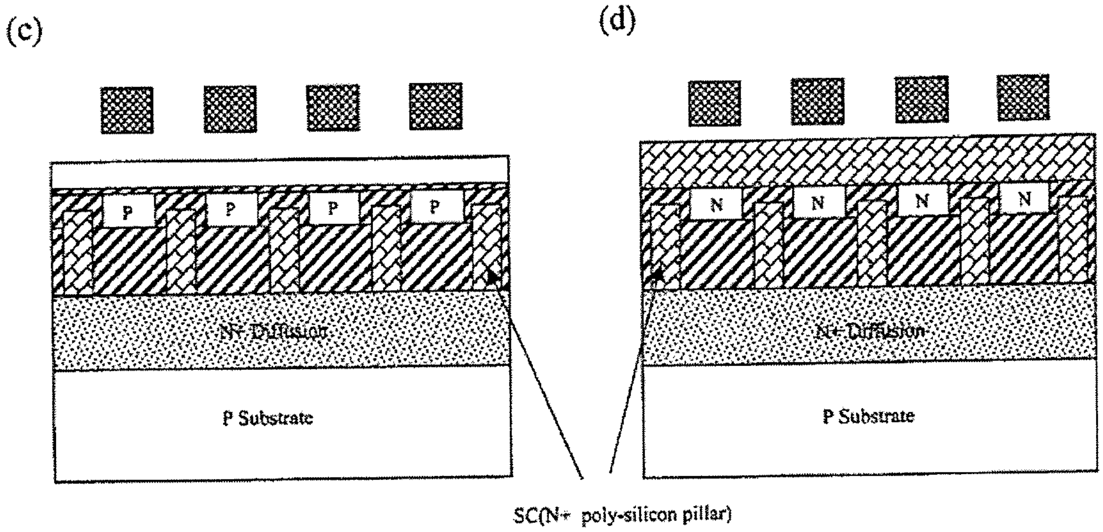
The Examiner argues that "Pham does not say the channel cannot be doped" and makes the unsubstantiated claim that "[t]he material of the substrate…used to form the fin could be doped material producing a doped channel." Examiner's Answer, page 8. Pham's disclosure indicates otherwise, because Pham states that "intense channel doping begins to degrade carrier mobility and junction characteristics" and because Pham does not disclose a single embodiment in which the channel of the FinFET is doped. Furthermore, Pham puts great emphasis in the disclosure on the method of annealing the amorphous silicon channel to increase the electron and hole mobility without the use of doping. Column 4, line 1 to column 5, line 20. In light of this evidence, the Examiner's argument that the channel of the FinFET of Pham would seemingly remain operable if doped because Pham does not explicitly say otherwise is unconvincing.

The Examiner also argues that Pham states that "the invention is not limited to any particular type of integrated circuit." Examiner's Answer, page 9. However, while this blanket statement of generally applicability indicates that it would be obvious to put the FinFET of Pham into any type of integrated circuit, it does not state or imply that it would be obvious to convert the transfer transistor FinFET taught by Pham into a storage transistor as suggested by the Examiner. Furthermore, Pham also goes on to state that "a polysilicon FinFET formed according to the teachings of the present invention may undergo or become part of a different or more complex fabrication process, provided, however, that the *essential characteristics of the present invention exist in the process*." Column 8, line 65 to column 9, line 14 (emphasis added). Therefore, it can be seen that Pham teaches away from changing the essential characteristics, such as maintaining an undoped channel.

The Examiner also argues that "intense doping…is not present or required in the partially depleted device of Ohsawa." Even assuming, *arguendo,* that this statement is true, the statement is still irrelevant. In the combined device envisioned by the Examiner, it is the FinFET of Pham that the Examiner claims must be doped, not the storage transistor taught by Ohsawa. Pham does not teach that the FinFET is or may be doped. The Examiner claims that the FinFET of Pham may be incorporated into the device of Ohsawa and that it may be lightly doped. However, The transistor of Ohsawa is designed "based on a one-transistor gain cell which is smaller…and more scalable to sub-01mm generations" and is useful at a size in which "short channel effects" are a problem in other transistors. Page 152, column 1. It is therefore clear that Ohsawa teaches a short gate length. Pham discloses that "[a]t reduced gate lengths, these [ultra thin-body MOSFETs] devices have difficulty in maintaining high drive currents…with low leakage" and that these problems are "typically overcome…by…highly doped channels." Column 1, lines 25-35. Therefore, it appears if the FinFET of Pham were to be doped at all, it would have to be heavily (i.e., intensely doped), and as discussed above, Pham teaches away from intense channel doping. Column 1, lines 33-35.

Aside for the problem of channel doping, the are other reasons that the FinFET of Pham cannot be combined with the storage transistor taught by Ohsawa to produce an operable transistor. For example, the storage transistor of Ohsawa is a "SOI" (silicon on insulator) transistor. Page 152, column 1. Pham teaches away from the use of a SOI substrate because it is "comparatively more expensive" and because "processing the FinFET device over an SOI substrate can yield only a single-layer device" due to "lithographic limits." Column 1, line 65 to column 2, line 2. Therefore, because Pham teaches a multi-layer device, Pham cannot be combined with the SOI storage transistor of Ohsawa. FIG. 4, layers 12, 32, 34, 22, and 38.

Also, the transistor of Ohsawa functions as a storage transistor with the aid of "[p]olysilicon pillars" which "stand inside the shallow trench isolation" and "serve as stabilizing capacitors (SCs) coupled to the body for enhancement of the signal and that of the retention time." Page 152, column 1 and FIG. 9.1.1(c) and (d) reproduced below. The FinFET of Pham teaches no such pillars. Nor is it obvious how such pillars could be removed from the substrate of Ohsawa and incorporated into the FinFET, why it would be obvious to do so, or how the FinFET could operate as a storage transistor with or without them. *See* Pham, FIG. 9 reproduced below.



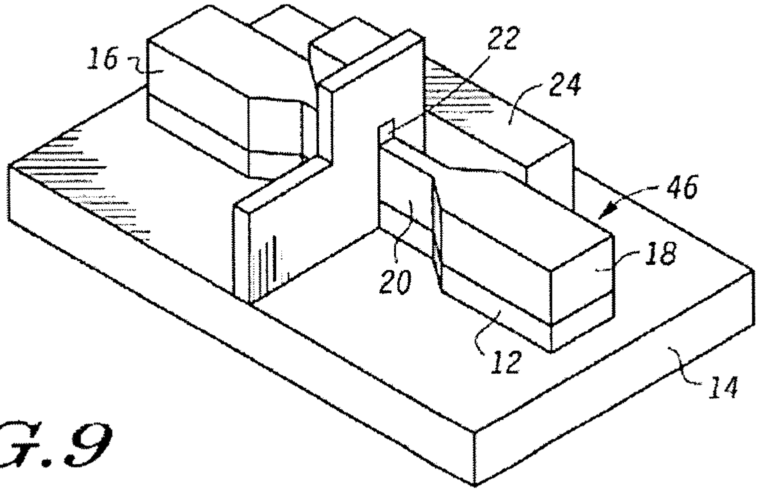


FIG.9

Clearly, the storage transistor of Ohsawa and the transfer transistor FinFET of Pham are complex and sophisticated devices and it would not be obvious to combine the FinFET of Pham with the device of Ohsawa as stated by the Examiner. In fact, as shown by the secondary considerations to the Graham factors in the above arguments, it would be seemingly impossible to combine the two. Appellant respectfully submits that this rejection is based improperly on hindsight and should be reversed.

2. Kencke does not cure the deficiencies of Pham or Ohsawa

The Examiner relies upon Kencke as allegedly teaching "generating carriers through impact ionization," and source/drain regions comprising "layers of Si_xGe_{1-x} and Se_yGe_{1-y} with different band gaps." The Examiner states that it would be obvious to combine Kencke with Pham and Ohsawa. As evidence, the Examiner only states that this combination would "provide better device characteristics." Examiner's Answer, page 11. The Examiner provides no insight into what characteristics would be better or how the combination of Kencke would make these characteristics better. This statement is not sufficient to show that the Examiner has considered the Graham factors, is not sufficient to show motivation to combine elements of complex devices such as transistors, and is not sufficient to show that the claims are obvious. In fact, this statement is so conclusory and perfunctory that it is only sufficient to show a blatant use of hindsight reasoning. As such, the rejection should be reversed.

IV. CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the claimed invention is not rendered obvious by the cited combination of references, and reversal of the final grounds of rejection is respectfully solicited.

Dated: June 20, 2007

Respectfully submitted,

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